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Design and Simulation of Convolution Using Booth Encoded Wallace Tree Multiplier

Jyoti Prakash Mohanty [1], Ritisnigdha Das [2], Siba Kumar Panda [2]
[1]*MTech Scholar, Dept of ECE, Centurion University of Technology & Management Bhubaneswar, Odisha*
[2]*Assistant Professor, Dept of ECE, Centurion University of Technology & Management Bhubaneswar, Odisha*

Abstract: *Convolution is one of the most used process in signal processing. In simple sense it is nothing but just flip then multiply and add. So the prime block in convolution is multiplication. Multiplication process is often used in digital signal processing systems, microprocessors designs, communication systems, and other application specific integrated circuits. Multipliers are complex units and play an important role in deciding the overall area, speed and power consumption of digital designs. Here in our proposed Wallace tree multiplier parameters like latency, complexity and power consumption has been improvised as compared to classical design. And hence the best possible convolution process has been realized.*

Keywords - *Booth encoder, MUX, SIPO, Wallace tree multiplier*

I. Introduction

Multipliers have gained a significant importance with the fundamentals of the digital computers. Multipliers are most habitually used in digital signal processing applications and microprocessors designs. In contrast to process of addition and subtraction, multipliers ingest more time and more hardware resources. With the recent advances in technology, a number of multiplication techniques have been employed for accomplishing the requirement of producing high speed, low power consumption, less area on a combination of them in one multiplier. Speed and area are the two major constraints which encounter each other. Therefore, it is the designer's assignment to decide proper balance in picking an appropriate multiplication technique as per needed. Parallel multipliers are the high speed multipliers. Therefore, the enriched speed of the multiplication operation is achieved using various schemes and anticipated Booth encoded Wallace tree is one of them. There are four phases in the multiplier architecture [1,2,3].

1. The first phase is booth encoder & 2's complement generator;
2. The second phase is the generation of partial products
3. Accumulation of partial product in third phase;
4. The fourth phase is the final addition phase.

II. Motivation

The motivation towards this work, is to form a Booth Encoded Wallace-tree multiplier[3,4]. Multipliers are one of the most important fragments in signal processing or other computationally concentrated applications[5,6]. Therefore, designing multipliers that are high-speed, low power, and consistent in layout are of substantial research interest. Many attempts have been made to reduce the number of partial products generated in a multiplication process by using the modified Booth algorithm. Moreover, Wallace Tree CSA [7,8] arrangements have been used to sum the partial products[10] in reduced time . In this regard, when both algorithms are combined in one multiplier, we can presume a significant reduction in computing multiplications. Our target is to reduce computation time by implementing Booth's algorithm for multiplication and to reduce chip area by spending Carry Save Adders arranged in a Wallace tree construction and at last stage we use a carry select adder to fasten the handling time.

III. Conventional Binary Multiplier Architecture

The multiplier is used in here is a 4-bit binary multiplier which receipts two four bit inputs and provides an 8-bit output. The binary multiplier which is used in convolution[9,11,13] here in the present project has a special characteristic that the inner carry will not be promoted to next stage. So the number of outputs obtained here is seven only because in binary multiplier the MSB is part is nothing but the carry obtained from the second MSB so as carry is not forwarded only seven bits will be obtained as output is taken .

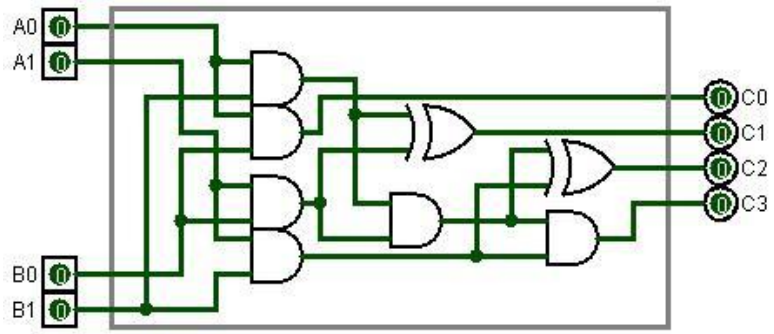


Fig.1. 2-bit Multiplier

IV. Proposed Wallace Tree Convoution Logic

The multiplier proceeds in two 8-bit operands: the multiplier (MR) and the multiplicand (MD), and create the 16-bit multiplication outcome of the two at its output. The architecture of the multiplier mostly consists of five major segments. They are: 2's Complement Generator, Booth Encoder, Partial Product Generator, Wallace Tree and Carry Look-ahead Adder. The multiplier has been created in its simplest conceptual form. We have used original Booth's Algorithm (Radix 2 encoding) for the Booth Encoder. The 2's Complement Generator implement a Ripple Carry Adder constructed from Full-adder modules. The Partial Product Generator employed two control signals x and z created by the Booth Encoder and uses these signals to indicate from and extend signs of '0', MD or -MD for creating 8 partial products. The 8 partial products are provided to Wallace Tree and added suitably. The Wallace tree uses both Full Adder and Half Adders. The final 16-bit intermediate results are added using a Carry Look-ahead Adder.

The Proposed Wallace Tree Architecture Multipliers are one of the most significant parts in signal processing or other computationally intensive applications. Therefore, creating multipliers that are high-speed, low power, and fixed in layout are of substantial research interest. Many efforts have been made to reduce the number of partial products generated in a multiplication method by using the modified Booth algorithm. Moreover, Wallace Tree CSA constructions have been used to sum the partial products in reduced time. In this regard, when both algorithms are shared in one multiplier, we can imagine a significant reduction in computing multiplications. Our objective is to reduce computation time by using Booth's algorithm [12]for multiplication and to reduce chip area by using Carry Save Adders arranged in a Wallace tree structure.The multiplier has M-bits X and N-bits Y as input and generate (M X N) bits output Z.

$$X = \sum_{i=0}^{M-1} X_i 2^i \quad \text{.....(1)}$$

$$Y = \sum_{j=0}^{N-1} Y_i 2^i \quad \text{.....(2)}$$

$$Z = X * Y = \sum_{i=0}^{M-1} \left(\sum_{j=0}^{N-1} X_i Y_i 2^{i+j} \right) \quad \text{.....(3)}$$

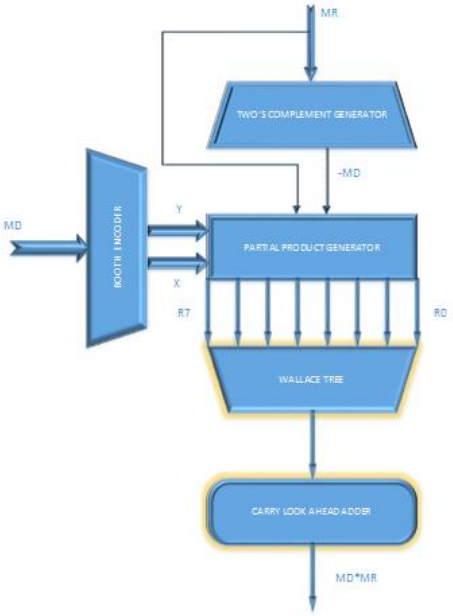


Fig.2. Proposed Wallace Tree Architecture

The output Z is calculated by sum of the partial product X_iY_J together. The easiest application requires an N-bit adder and take M cycles to produce the output. Another implementation of multiplier is so called adder array multipliers which accomplish greater speed at the cost of larger hardware. Numerous other technologies have been developed to improve the speed and decrease the power consumption of multiplier. There are two widely used approaches: booth algorithm and Wallace tree compressor. Booth algorithm can perform multiplication on both non-negative and negative operands by using 2's complement number. Moreover, the booth algorithm can further reduce the number of partial product which can lead to substantially delay and area reduction. This can be demonstrated by the following example.

$$\mathbf{x = \sum_{1=0}^{m-1} xi2^1 = \sum_{k=0}^{n} \binom{n}{k} x^k a^{n-k} 2i} \quad \text{.....(4)}$$

Where X is the multiplicand. Mr*Md was selected, and the implementation for 4x4 was prepared in order to have short convolutions that will lead to the lowermost implementation cost .The circuit works with two signals having N values each. They selected Mr=4 in this implementations. Which consider the two numbers like two arrays having four locations each to store values. Each array is input to a quadruple 4X1 Mux separately. Hence they can have each signal value up to 4 bit. The basic concept of convolution is to flip, multiply and add. Now for two signals of four values each, we have to flip (invert one of the signals) multiply and then add the values.

The block diagram of overall convolution Process is shown in Fig.3. which states the flipping of the values is completed by selection of the 4X1 Multiplexer. The output data from the multiplexer is applied to the serial input parallel output block the data will be converted serial to parallel. The output of the SIPO block is connected to the Booth encoded Wallace tree multiplier. Then the data will be stored in the registers. In this design we did some change in our multiplier to achieve the higher speed.

The multiplier which we are using is Wallace tree multiplier in this we have to change the carry propagation routine because in convolution process's direct method, carry is not shifted and added towards left all the column are added together separately. So we got 7 outputs. In Fig.3 overall convolution process is shown.

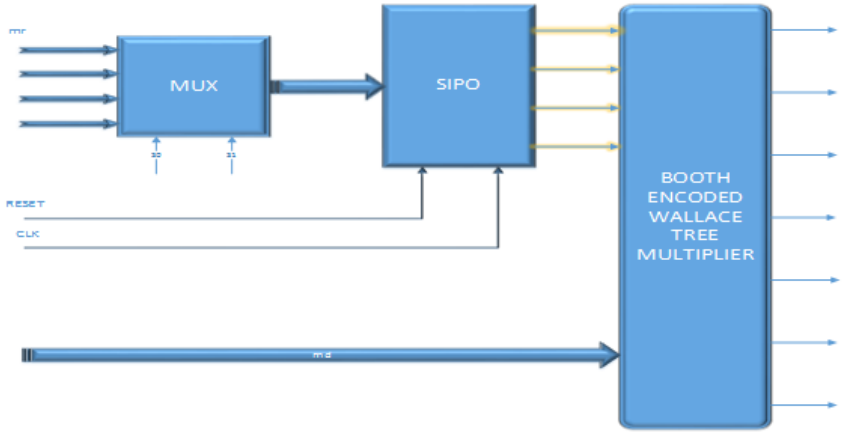


Fig. 3 Overall convolution process

V. Result Analysis And Discussion

Fig.4. Power Analysis Report

Above figure shows total power consumption by the designed convolution logic using Xilinx Xpower analyzer. And it is found to be supply power of 0.033watt and dynamic power.002watt which is very less as compared to existing convolution architecture having 2 MUX and 2 SIPOs.

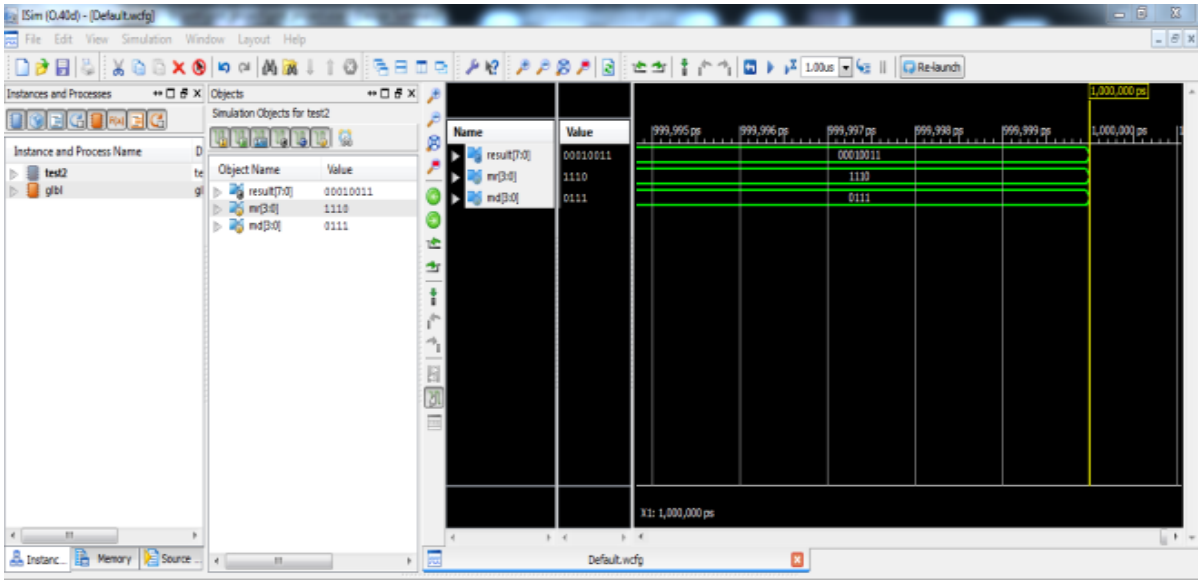
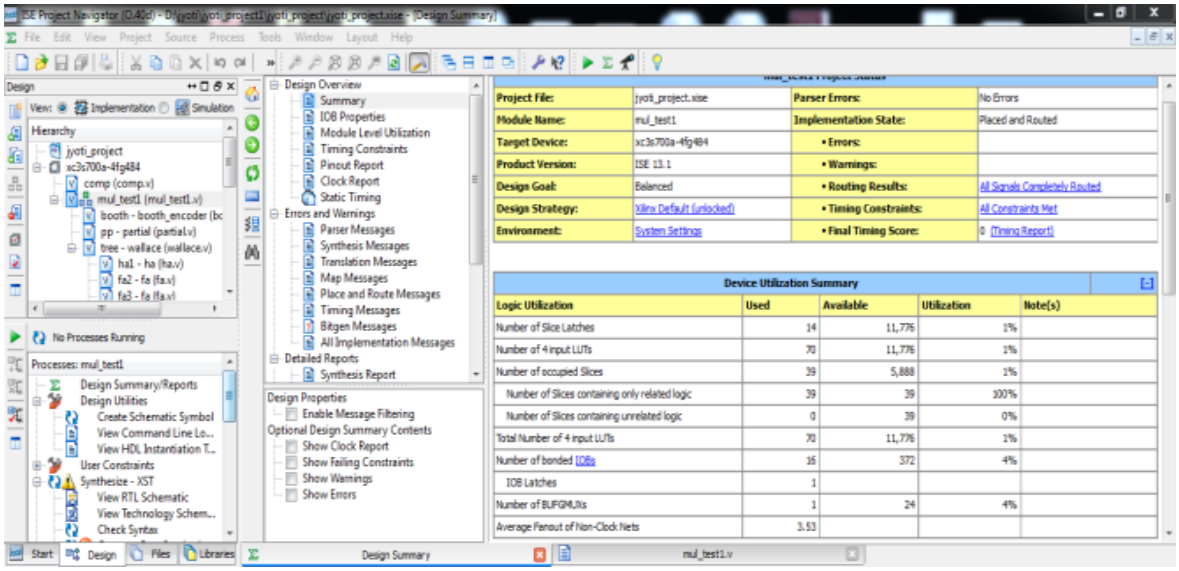


Fig.5 Output waveform

Convolution result has been shown in above figure for two inputs 1110 and 0111. Which is found to be 00010011.



Project File:	jyoti_project.xise	Parser Errors:	No Errors
Module Name:	mul_test1	Implementation State:	Placed and Routed
Target Device:	xc3s700a-4fg484	• Errors:	
Product Version:	ISE 13.1	• Warnings:	
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Latches	14	11,776	1%	
Number of 4 input LUTs	70	11,776	1%	
Number of occupied Slices	39	5,888	1%	
Number of Slices containing only related logic	39	39	100%	
Number of Slices containing unrelated logic	0	39	0%	
Total Number of 4 input LUTs	70	11,776	1%	
Number of bonded IOBs	16	372	4%	
IOB Latches	1			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.53			

Fig.6. Synthesis Report

Finally designed summary has been shown that clearly shows better fan out and less number of LUTs used.

VI. Conclusion

The designed Booth encoded Wallace tree multiplier is coded using Verilog HDL and the desired product is achieved with the help of less number of partial products. So of course less area and less power consumption is achieved. The designed Wallace tree is then used in convolution algorithm which is again improvised by reducing number of multiplexor and shift registers.

The improvement in power efficiency and chip area in terms of I/O pins and no. of LUTs best describes the application of such a noble architecture to be used with many of the circuits as almost all electronics circuits' process data using convolution. In future we will try to develop such a convolution IP which can be used by other researchers.

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